Design Notes

Intricacies of 80C51 Ports

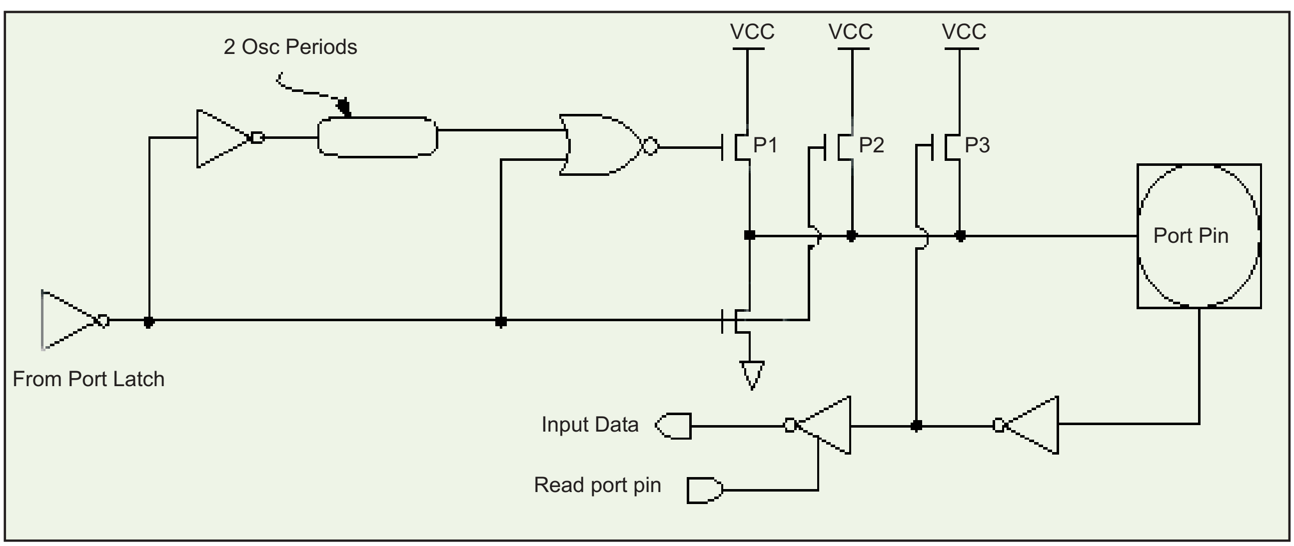
80C51 microcontroller ports are open drain FETs, with or without an internal pullup resistor. This edition of Design Notes focuses on 80C51 port lines and explains some traps the designer should be aware of when using them. We look at the behaviour of quasi-bidirectional lines, the different types of pullup resistors inside the chip, power supply latch up and how software "read-modify-write" instructions operate.

Introduction to 80C51 I/O Ports
80C51 I/O ports are usually one of two types.

Firstly they can be Open Drain FETs. Each port line has an internal FET whose drain is connected to the port pin of the microcontroller and whose source is connected to ground. The FET's operation is controlled by a latch. When a "0" is written to the latch, the FET is turned on and pulls the drain pin down to ground. When a "1" is written to the latch, the FET is turned off and a high impedance is seen at the port pin.

The second type of port line is also an open drain FET but with the addition of an internal pullup resistor tied to the FET's drain. When a "0" is written to the latch, the FET is turned on and pulls the port line to ground (same as described above). When a "1" is written to the register, the FET is turned off and the pullup resistor drags the port pin up to VCC. This type of port pin is called quasi-bidirectional because unlike the open drain FET which is a true bidirectional port, this has a pullup resistor.

Both types of port lines can be used as inputs and outputs. If they are used as outputs, they operate as described above. If they are used



CMOS Configuration
pFET1 is turned on for 2 oscillator periods after output makes "0" to "1" transition. During this time, pFET1 also turns on pFET3 through the inverterting FET to form a latch which holds the "1".pFET 2 is also on.

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as inputs, a sensing circuit inside the 80C51 will read the status of the port line and transfer it to a read register, to be read by software.

To use them as inputs, the FET must be turned off by writing a "1" to the port latch. This prevents the FET crowbarring external circuitry connected to the port pin.

Further information on 80C51 port architectures can be found in reference (2).

This is an example of a major difference between 80C51 and 68HC05 controllers. The latter has a separate register for setting up each port line as an input or output. This is called a Data Direction Register. 68HC05 ports are usually a push pull configuration when used as outputs and have a high impedance when used as inputs (i.e. no pullup resistor).

80C51 Pull Up Resistors
The pullup resistor inside a quasi-bidirectional port is usually of the order of 50k-100k impedance and will not load the outside circuitry if the port is used as an input. The pullup is in fact a FET rather than a resistor and it has a large impedance connected to VCC.

There are three types of pullup resistors inside a quasi-bidirectional port. The "very weak" pullup is on at all times and has a maximum source current of 50μA. The "weak" pullup is active when the port write register is a "1" and the port pin is actually high. It has a minimum source current of 60μA. The "strong" pullup is active for two clock cycles whenever the port write register changes from a "0" to a "1". The aim of the strong pullup is to reduce the risetime on the port pin when the port changes from low to high especially with highly capacitive loads.

The figure on page 1 shows the 80C51 port architecture. pFET1 is the strong pullup. pFET2 is the very weak pullup and pFET3 is the weak pullup which is on while the port pin is "1".

Strength Of the Strong Pull Up Resistor
How strong is the strong pullup? None of the 80C51 databooks clearly specify the strength of this resistor. The Philips databook states it "is approximately 100 times stronger than a weak pullup", thus making it approximately 500 ohms. Some measurements were done by Electronics By Design using an 80C51 controller and found it to be able to supply 15mA when shorted directly to ground i.e. it's impedance was 333 ohms (5V/15mA). Other devices such as a Philips 87C751 can supply 2-3 times this current.

Tricks 'n' Traps To Watch Out For
Quasi-Bidirectional Ports Dragged Low
When loading a port pin the designer must be aware of the internal pullup's resistance if it will be used to pull the port line high.

Say the port line is used as an output. If a relatively low impedance to ground is connected externally to the port pin and a "1" is written to the port latch, it's possible the port line will be dragged low at all times and a "high" may never be seen. Let's say the net effect of the internal pullups is a 50k resistance to VCC and the outside circuitry has a 10k resistor to ground at the port pin. If a "1" is written to the port latch, the FET will be turned off and the output voltage on the port pin will be the resistive division of 10k and 50k i.e. 0.83V. In other words the port line will never go above this voltage and will be constantly low.

A similar situation can occur if the port line is connected directly to the base of an NPN transistor (whose emitter is grounded) and the internal pullup resistor is used to source current into the base. If the state of the port line is read by the software to determine whether the transistor is on or off, the port line will always read "0" because it will never rise above 0.65V (Vbe) since the BE junction of the transistor will clamp it at this voltage.

Power Supply "Latch-up"
Imagine the following situation. An 80C51 controller is powered up. Immediately on power up (and before the power-on reset circuitry takes over) many of the port lines are "0". In fact any number of them could be "0" or "1" as this is a totally random situation. The power-on reset circuitry takes over and forces all port lines to "1". By doing so, the strong

pullups are activated hence many lines are simultaneously drawing a high current for two oscillator periods. Factor in a weak power supply, and you have the scenario where the VCC rail of the processor may not rise to 5V and the processor will not start.

This situation would not normally occur except in applications with a weak power supply, such as remote telemetry actuators which share power supply and data cabling, or line powered RS232 links. Any application with more than a few ohms of impedance in the microcontroller's power supply lines will be susceptible. A similar result can occur if the software changes an entire group of 8 port lines from "0" to "1". The moral of the story is to ensure the power supply has sufficiently low impedance to prevent this happening.

<u>High Load Capacitance</u>
As mentioned earlier, the strong pullup resistor engages on a "0" to "1" transition of the port pin and is activated for two oscillator clock periods. The threshold voltage of activation is 2.0V on a rising port pin edge.

Assume a port pin is used as an output and is at "0" state, thus it's output FET is turned on. Typically with a reasonably high impedance load (say driving an external medium power FET) the port pin voltage will be virtually 0V. When a "1" is written to the port latch, the 80C51 port FET will be turned off. For the duration of time from this point to the time it rises to 2.0V (the strong pullup threshold) the only thing pulling the pin high is the very weak pullup whose impedance is typically 50k-75k. If the port pin has significant capacitive loading (say 10nF) it will take approximately hundreds of microseconds until the 2.0V threshold is reached and the strong pullup is activated. Even if a lower capacitance such as 1nF is present it will still take microseconds which equates to a few instruction cycles of the processor. The simple cure for this problem is the use of an external pullup resistor to VCC with a much lower impedance than the internal pullups.

It can be seen from this example the designer must keep in mind the high impedance of the pullup resistors.

Read-Modify-Write Instructions
Some 80C51 instructions read a port latch and others read a port pin. The question is which instructions do the former and which do the latter? The instructions which read a value, then modify it, then write it back, all read this value from the latch rather than the pin and write the result into the latch. They are called read-modify-write instructions and include ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ, MOV Px.y,C, CLR Px.y and SETB Px.y. All other instructions read the pin rather than the port latch.

The reasoning for this is to alleviate the problem mentioned earlier where a port pin pullup resistor is used to drive the base of a transistor. By reading the latch, a correct result is obtained as to whether the port pin is "0" or "1". If the pin were read, the result would always come back as "0".

Further information on "read-modify-write" instructions can be found in reference (2).

References and Acknowledgments

(1) Everything You Never Wanted to Know About 80C51 I/O Ports.
Signetics Microcontroller Applications Newsletter - Q1 1991
Philips Semiconductors
(2) 80C51 Based Microcontrollers Databook - 1997
Philips Semiconductors
(3) 80C51 Application Notes 1997
Philips Semiconductors